REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1-14 and 16-35 are currently active in this case. Claims 4, 6-9, 14, 16, 18, and 19 have been amended; Claim 15 has been canceled and Claims 27-35 have been added by way of the present amendment. New Figs. 7 and 8 have been added, and the specification has been amended. Each new and amended claim, figure, and changes to the specification are supported by the specification and claims as originally submitted and no new matter has been added.

In the outstanding Official Action, the drawings and Claims 6, 16 and 18 were objected to; Claim 15 was rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement; Claims 4-8 and 15-19 were rejected under 35 U.S.C. §112, second paragraph as being indefinite; Claims 1-5, 7, 9, and 13-19 were rejected under 35 U.S.C. §102(e) over *Alpert et al.* (U.S. Patent Publication No. 2002/0184607, hereinafter *Alpert*); Claims 1-5, 7, 9, and 13-19 were rejected under 35 U.S.C. §102(e) over *Van Ginneken* (U.S. Patent No. 6,453,446); Claims 1-5 and 13-19 were rejected under 35 U.S.C. §102(b) over *Le* (U.S. Patent No. 5,995,735); and Claims 1-5, 7, 9, and 13-19 were rejected under 35 U.S.C. §102(e) over *Boyle et al.* (U.S. Patent Publication No. 2001/0010090, hereinafter *Boyle*).

Applicants appreciatively acknowledge the identification of allowable subject matter in Claims 6, 8, and 10-12.

Applicants have submitted herewith new Figs. 7 and 8, and amended corresponding portions of the specification to reflect the new figures. Fig. 7 is an example block diagram of a physical hierarchy of a circuit design with placed macros 720. Figure 8 is an illustration of a method of the present invention embodied in a set of computer readable instructions stored on a computer readable

media. Applicants respectfully note that the new figures are supported in Applicants original specification and claims (e.g., placed macros at page 7, lines 22-23, claim 1; computer readable instructions and media in Claims 13-15 and 24-26, plus discussions throughout Applicants specification in which those items are clearly inherent, including "design automation toolkit," on page 5, line 5). The corresponding amended portions of the specification accommodate the new drawings, and the new drawings and specification amendments directly reflect the above cited portions of Applicants specification and claims as originally submitted. Accordingly, Applicants respectfully submit that no new matter has been added, and further request that the objections to the drawings be withdrawn.

Applicants have amended certain of the claims to improve clarity and/or correct typos. It is believed that the clarifications also render moot the rejections under 35 USC 112 2nd paragraph. Accordingly, Applicants request that those rejections be withdrawn.

Applicants respectfully traverse the rejection of Claim 1, under 35 USC 102(e) as being anticipated by *Alpert*. Claim 1 recites:

> ***1. (Original) A method of inserting buffers in a circuit design, comprising the steps of:***
>
> ***preparing a physical hierarchy of the circuit design with placed macros;***
>
> ***performing global routing on the physical hierarchy;***
>
> ***determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets;***
>
> ***calculating a position for each buffer; and***
>
> ***inserting a buffer configured to boost timing performance at each calculated position.***

However, *Alpert* fails to teach or suggest similar subject matter.

Applicants respectfully note that *Alpert* is a system that modularizes a design into a set of tiles (e.g., tile graph, Figs. 4/5, et al.) and then buffer locations are inserted in the tiles based on buffer needs of nets (Abstract, line 8). The nets themselves are then routed through the tiles and buffer locations (Summary of the Invention, lines 9-10). Applicants respectfully admit that *Alpert* includes discussion of macros and global routing, but none of that teaches or suggests Applicants' recited invention.

Applicants respectfully traverse the assertion in the outstanding Office Action that indicates *Alpert's* paragraphs 7 and 48 teach Applicants' claimed step of *"determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets."* More specifically, paragraph 7 describes a use of buffers in circuit design, that being "the need for interconnect-centric design methodology" (paragraph 7, lines 1-4); Insertion of buffer blocks into feasible regions (paragraph 7, lines 5-12); optimization congestion relief (paragraph 7, lines 12-14); maximizing buffer insertion (paragraph 7, lines 14-18); and multi-commodity flow based buffer insertions (paragraph 7, lines 18-22). However, none of this indicates the recitation of a number of buffers to be inserted on each edge of global routing nets or insertion of buffers at the edge of global routing nets to boost timing performance.

Regarding *Alpert's* paragraph 48, a description of tiling is described along with formulas for determining wire and buffer congestion. As to wire congestion, *Alpert* suggests a comparison to a maximum allowable wire congestion. However, *Alpert* is silent on whether buffer congestion is utilized to indicate insertion of additional buffers at the edge of global routing nets to boost timing performance. Nevertheless, paragraph 49 goes on to discuss planning to assure a single buffer or driver does not connect to too many sinks. However, such an analysis is not to determine buffer insertion at global routing net edges to boost timing performance.

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embodied in a set of computer readable instructions stored on a computer readable media. Applicants respectfully note that Figures 7 and 8 are supported in Applicants original specification and claims (e.g., placed macros at page 7, lines 22-23, claim 1; computer readable instructions and media in Claims 13-15 and 24-26, plus discussions throughout Applicants specification in which those items are clearly inherent, including "design automation toolkit," on page 5, line 5). The corresponding amended portions of the specification accommodate Figures 7 and 8, and directly reflect the above cited portions of Applicants specification and claims as originally submitted. Accordingly, Applicants respectfully submit that no new matter has been added, and further request that the objections to the drawings be withdrawn.

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driver does not connect to too many sinks. However, such an analysis is not to determine buffer insertion at global routing net edges to boost timing performance.

Applicants respectfully note that *Alpert* provides examples of various iterations of buffer and routing design. To that end, *Alpert* does utilize maximum and average buffer congestion for analysis along with other traditional parameters such as wirelengths, net delays, etc (paragraph 55). However, *Alpert's* buffer congestion parameters are only averages and other statistical information for what is available for a tile (e.g., paragraph 055), and their distribution is not specific as in an insertion for boosting timing performance. Instead, the distributed buffers are utilized as needed for interconnections (e.g. paragraphs 007, 008, 011, 043) and particularly in a predetermined distribution through the tile (e.g., algorithmic based distribution, congestion based cost algorithms (paragraph 63), etc.). Further, the overall strategy by *Alpert* is different than that which is accomplished by the present invention. *Alpert* mainly looks to relieving congestion through uniformity, and the present invention boosts existing performance through additional buffer insertions.

Finally, *Alpert* utilizes existing buffer locations for the assignment of buffers, which are then used for routing nets (Abstract, lines 8-11), however, the present invention inserts buffers after routing, not for completing a design, but to improve performance of the existing layout.

Regarding the assertion of *Alpert's* insertion of buffers (e.g., paragraphs 005, 007, and 043), Applicant respectfully disagrees. Applicants' claimed invention is performed after, or in immediate conjunction with global routing ...(i.e., the buffers are inserted after global routing, and specifically to boost the then existing performance of the system). Further, Applicants respectfully note that *Alpert's* paragraph 007 is specifically related to interconnects and other non performance boosting operations. Paragraph 005 actually teaches away from the

present invention by citing backend buffer insertions as causing difficulties in timing closure (however, Applicants' buffer insertion is at the back end of the design process as it is for enhancing, or boosting, performance of the circuit). And finally, paragraph 043 also only describes interconnect-centric processes that have not yet completed global routing In contrast, *Alpert* fails to take an existing design and boost performance. Instead, *Alpert* works to make a design work, and then, if performance is to be increased, the entire design is reshuffled – see paragraph 060 *"Instead of ripping up nets in congested regions, we rip-up and re-route* ***every*** *net ..." (emphasis added)*.

Applicants also respectfully note *Alpert's* discussion of buffer insertion at paragraph 065 and others. However, that discussion is strictly related to insertion based on a per tile cost of inserting the buffer for use in building a net or other connections not related to making a performance boost of an existing net.

Therefore, Applicants respectfully note that Claim 1 cannot be anticipated by *Alpert* because *Alpert* fails to teach or suggest subject matter specifically claimed in Claim 1. Accordingly, Applicants respectfully submit that Claim 1 is patentable over *Alpert*.

Applicant also respectfully traverses the rejection of Claim 1 as being anticipated by *Van Ginneken*. Applicants respectfully traverse the assertion in the outstanding Office Action that equates *Van Ginneken's* buffer determinations (col. 13, lines 24-36) to Applicants' claimed "*"determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets."*

In particular, Applicants respectfully note the discussion at col. 13 in *Van Ginneken* related to Fig. 8. *Van Ginneken's,* Fig. 8, describes a process whereby buffers are inserted into a design, however, the buffers are inserted only in

locations where they can be inserted without increasing network delay. More importantly, the criteria for evaluating whether or not a buffer will be inserted is an area based analysis (e.g., step 665). Col. 13 recites *"...locations in the circuit are determined where a buffer can be added so that buffer insertion will still permit timing constraints to be met."* However, that is entirely different than Claim 1's determining a number of buffers inserted for boosting timing performance. more specifically, *Van Ginneken's* buffer insertions are dependent upon space, not timing requirements (e.g., step 665, Fig. 8, and col. 13, lines 51-53 *"...the buffer is inserted if the impact on the circuit area is positive ..."*). Thus *Van Ginneken's* buffer insertion is very similar to that discussed above with respect to *Alpert*, buffers that have a good impact on congestion or available circuit real estate are either utilized, assigned, or inserted). However, the references fail to discuss Applicants' recited Claim 1 related to determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets.

Therefore, Applicants respectfully note that Claim1 cannot be anticipated by *Van Ginneken* because *Van Ginneken* fails to teach or suggest subject matter specifically claimed in Claim 1. Accordingly, Applicants respectfully submit that Claim 1 is patentable over *Van Ginneken*.

Applicants respectfully traverse the rejection of Claim 1 as being anticipated by *Le*. Applicants respectfully note that *Le* describes a method for placement of repeaters or buffers in a design. In particular, *Le's* placement of repeaters is designed to minimize wire run lengths from an insertion point in a net to the actual repeater (*Le*, col. 1, lines 50-52, discussing the problem to be addressed). To that end, *Le* locates optimal virtual locations for buffer placement, and then runs global routing through the optimally placed buffers. However, the present invention in Claim 1 specifically claims *"determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets;"*

And, therefore, Claim 1 is a recitation of inserting buffers on the net that is different and neither taught nor suggested by *Le's* buffer placement and then building the net through the buffers in a subsequent global routing. Accordingly, Applicants respectfully submit that Claim 1 cannot be anticipated or even suggested by *Le.*

Applicants respectfully traverse the rejection of Claim 1 under 35 USC 102 as being anticipated by *Boyle*. Applicants respectfully traverse the assertion in the outstanding Office Action that indicates *Boyle* paragraphs 0038 and others teach Applicants' claimed step of *"determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets;"* Applicants admit that *Boyle* provides for the insertion of inverter pairs (or buffers) in a design. However, *Boyle's* criteria for buffer insertion is related to load management and/or standard designs using buffers. For example, discussion in *Boyle's* paragraph 0038 includes *"... alternative implementations of logic circuits and insertion of deletion or signal buffers,"* Further, *Boyle's* design changes are for either the preservation of logic element placements and/or load management (e.g., capacitive load management) on the circuits. Paragraph 0045 provides buffer insertion for preservation of logic element placements, and Paragraph 0055 begins a lengthy discussion of load management (e.g., based on fan-out, paragraph 61; Capacitive load management, paragraph 0044, load calculations/load shielding, paragraph 0080). And, none of this indicates buffer insertion for boosting timing. That some of the same or all of the same consideration may be utilized in Applicant's claimed invention to determine timing boosting buffer insertions (e.g., load calculations and fan-out, as indicated in dependent claim 8) does not mean that *Boyle's* load management is done in a manner to boost timing. In fact, *Boyle* makes no such assertions.

The remaining cited paragraphs of *Boyle* discuss either candidates for insertion or virtual placements of inverter pairs (*"virtual buffer,"* paragraph 0060; *"likely candidates for insertion,"* paragraph 0095; Virtual Inserter Pairs (VIPs),

paragraphs 0105). However, these virtual buffers are not intended to dictate placement of actual buffers on the edges of nets, as they are merely placeholder (*"virtual buffers"*) so that timing is improved during design periods where other portions of the design are being optimized. Once that optimization is completed, *Boyle's* virtual buffers are no longer needed and they simply go away (virtual buffers that were not there to start with, are removed) (e.g., *"Moreover, as the partitioning continues, a large portion of these nets will become shorter such that the VIPs are removed,"* paragraph 0105.) In contrast, the present invention specifically claims the insertion of buffers, not virtual buffers used as a temporary (or "virtual") placard.

Even in cases where the virtual buffers are not removed, the buffers are not placed until lower levels of design, and prior to solidification of global routings (paragraph 0106, last sentence). Moreover, *Boyle's* discussion admits that actual insertion of buffers would be a ***crude specification*** of global routing (paragraph 0104, first sentence, emphasis added, indicating that the buffers are not actually intended to be inserted). In contrast, Applicants' claimed steps of determining a number of buffers, and then inserting, are performed after global routing.

Therefore, Applicants respectfully submit that *Boyle* is devoid of any practical discussion that would teach or suggest Applicants' claimed step of *"determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets;"* and other claim elements directly related thereto, such as the insertion of these specific buffers, and, Applicants respectfully submit that Claim 1 is patentable over *Boyle*. Accordingly, Applicants further respectfully submit that Claim 1 is patentable over the cited art of record.

New independent claims 27, 29, and 31 each include patentably distinguishing subject matter applicable to the above discussion and/or similar to the subject matter already identified as being allowable, and are also respectfully

submitted as being patentable over the cited art. Based on the patentability of Claims 1, 27, 29, and 31, Applicants further respectfully submit that dependent Claims 2-19, 28, 30, and 32-35 are also patentable.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,
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Dated: 6/14/2005

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In the Drawings:

The attached sheet of drawings include new Fig. 7 and new Fig. 8.